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10/691,650	10/24/2003	Takahiro Fukuhara	244424US6	7632

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
WANG, CLAIRE X	

ART UNIT	PAPER NUMBER
2624	

NOTIFICATION DATE	DELIVERY MODE
05/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/691,650	FUKUHARA ET AL.	
	Examiner	Art Unit	
	Claire Wang	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 9-29 are rejected under 35 U.S.C. 102(b) as being anticipated by International Standard, Information technology – JPEG 2000 image coding system (ISO/IEC 15444-1).

As to claim 1, International Standard, Information technology – JPEG 2000 image coding system (from this point forward shall be referred to as ISO/IEC) teaches An image encoding apparatus (JPEG 2000 image coding system, page 1, title) comprising: filtering means (low-pass and high-pass filter, section F.2) for generating a plurality of subbands (section B.5), and applying hierarchical filtering (levels are associated with each subband, section B.5), to the sub-bands. ISO/IEC also teaches code block generating means for splitting the subbands generated by said filtering means for generating a plurality of code blocks (section B.7) each being of a predetermined size (code block size is determined by precinct size, section B.7); bitplane generating means (Annex D) for generating a plurality of bitplanes (Fig. D-1) from the most significant bit to the least significant bit (section D.2.1), in terms of said code block as a unit; encoding object predicting means for predicting the number of bitplanes for encoding (predicting could be interpreted two different ways. First, one

may interpret predicting to be codestream termination, which is when we know how much bandwidth is available to us and terminating the codestream when the limit has been reached. This is in away predicting how much data we can compress. Annex D, section D.4 The second way is to interpret predicting as the region of interest. Then we are able to predict and know how much data to send or not to send by knowing the region of interest. Annex H), as object of the encoding, and for extracting, from an upper bit side of each code block, a number of bitplanes corresponding to the predicted number of bitplanes for encoding (by knowing the above discussed information we would be able to predict how much date to send; section D.4 and Annex H); bit modeling means (significance propagation; section D.3.1) for performing bit modeling from one bitplane extracted by said encoding object predicting means to another (Fig. D-2 demonstrates the different bit models, using surrounding neighbor coefficients we are able to create a context vector that can predict different likely values in the bitplane); encoding pass generating means (selective arithmetic coding bypass, section D.6) for generating an encoding pass from one bitplane to another (Table D-9 teaches of the different types of passes with corresponding coding operations and bit-plane numbers) arithmetic coding means (arithmetic entropy coding, Annex C) for performing arithmetic coding in the encoding passes generated by said encoding pass generating means (Annex C); code volume controlling means (rate control, section J.14) for controlling the code volume, based on arithmetic codes generated by said arithmetic coding means, so that a target code volume will be reached; and packet generating means (packet header information coding, section B.10) for appending a header to the arithmetic codes

controlled as to code volume by said code volume controlling means, to generate a packet (section B.10).

As to claim 10, it differs from claim 1 in that claims 1 is an apparatus claim whereas claim 10 is a method claim. Therefore claim 10 is analyzed in the same way as claim 1.

As to claim 12, it differs from claim 1 in that claims 1 is an apparatus claim whereas claim 12 is a program. Therefore claim 12 is analyzed in the same way as claim 1.

As to claim 14, it differs from claim 1 in that claims 1 is an apparatus claim whereas claim 14 is a computer readable medium. Therefore claim 14 is analyzed in the same way as claim 1.

As to claim 9, ISO/IEC teaches an image encoding apparatus comprising (JPEG 2000 image coding system, page 1, title): filtering means (low-pass and high-pass filter, section F.2) for generating a plurality of sub-bands (section B.5), and applying hierarchical filtering to the sub-bands (levels are associated with each subband, section B.5); code block generating means for splitting the subbands generated by said filtering means for generating a plurality of code blocks (section B.7) each being of a predetermined size (code block size is determined by precinct size, section B.7); bitplane generating means (Annex D) for generating a plurality of bitplanes (Fig. D-1) from the most significant bit to the least significant bit (section D.2.1), in terms of said code block as a unit; encoding object predicting means for predicting the number of encoding passes for encoding (predicting could be interpreted two different ways. First,

one may interpret predicting to be codestream termination, which is when we know how much bandwidth is available to us and terminating the codestream when the limit has been reached. This is in away predicting how much data we can compress. Annex D, section D.4 The second way is to interpret predicting as the region of interest. Then we are able to predict and know how much data to send or not to send by knowing the region of interest. Annex H), as object of the encoding, for generating the information on the number of the encoding passes (by knowing the above discussed information we would be able to predict how much date to send; section D.4 and Annex H); bit modeling means (significance propagation; section D.3.1) for performing bit modeling from one bitplane to another; encoding pass generating means for generating encoding passes from one bitplane to another (Fig. D-2 demonstrates the different bit models, using surrounding neighbor coefficients we are able to create a context vector that can predict different likely values in the bitplane); encoding pass generating means (selective arithmetic coding bypass, section D.6) for generating an encoding pass from one bitplane to another (Table D-9 teaches of the different types of passes with corresponding coding operations and bit-plane numbers);arithmetic coding means (arithmetic entropy coding, Annex C)for performing arithmetic coding only on a number of the encoding passes, afforded by the information on the number of encoding passes, as counted from the most significant bit side of each code block, from among the encoding passes generated by said encoding pass generating means (Annex C); code volume controlling means (rate control, section J.14) for controlling the code volume, based on an arithmetic code generated by said arithmetic coding means, so that a

target code volume will be reached; and packet generating means (packet header information coding, section B.10) for appending a header to the arithmetic code, controlled as to code volume by said code volume controlling means, to generate a packet (section B.10).

As to claim 11, it differs from claim 9 in that claims 9 is an apparatus claim whereas claim 11 is a method claim. Therefore claim 11 is analyzed in the same way as claim 9.

As to claim 13, it differs from claim 9 in that claims 9 is an apparatus claim whereas claim 13 is a program. Therefore claim 13 is analyzed in the same way as claim 9.

As to claim 15, it differs from claim 9 in that claims 9 is an apparatus claim whereas claim 15 is a computer readable medium. Therefore claim 15 is analyzed in the same way as claim 9.

As to claim 16, ISO/IEC teaches an image encoding apparatus comprising: filtering means (low-pass and high-pass filter, section F.2) for generating a plurality of sub-bands (section B.5), and applying hierarchical filtering (levels are associated with each subband, section B.5) to the sub-bands; code block generating means for splitting the subbands generated by said filtering means for generating a plurality of code blocks (section B.7) each being of a predetermined size (code block size is determined by precinct size, section B.7); bitplane generating means (Annex D) for generating a plurality of bitplanes (Fig. D-1) from the most significant bit to the least significant bit (section D.2.1), in terms of said code block as a unit; bit modeling means (significance

propagation; section D.3.1) for performing bit modeling from one bitplane to another (Fig. D-2 demonstrates the different bit models, using surrounding neighbor coefficients we are able to create a context vector that can predict different likely values in the bitplane); encoding pass generating means (selective arithmetic coding bypass, section D.6) for generating an encoding pass from one bitplane to another (Table D-9 teaches of the different types of passes with corresponding coding operations and bit-plane numbers); arithmetic coding means (arithmetic entropy coding, Annex C) for performing arithmetic coding in the encoding pass generated by said encoding pass generating means (Annex C); code volume controlling means (rate control, section J.14) for controlling the code volume, based on an arithmetic code generated by said arithmetic coding means, so that a target code volume will be reached; and packet generating means (packet header information coding, section B.10) for appending a header to the arithmetic code, controlled as to code volume by said code volume controlling means, to generate a packet; wherein in said code volume controlling step, said arithmetic codes are summed in a sequence from the arithmetic code with the highest bit position in the totality of the code blocks of said input picture to the arithmetic code of the lowermost bit, from one bitplane to another or from one code pass to another, and summation is halted when a preset target code is exceeded (section B.10).

As to claim 19, it differs from claim 16 in that claims 16 is an apparatus claim whereas claim 19 is a method claim. Therefore claim 19 is analyzed in the same way as claim 16.

As to claim 20, it differs from claim 16 in that claims 16 is an apparatus claim whereas claim 20 is a program. Therefore claim 20 is analyzed in the same way as claim 16.

As to claim 21, it differs from claim 16 in that claims 16 is an apparatus claim whereas claim 21 is a computer readable medium. Therefore claim 21 is analyzed in the same way as claim 16.

As to claim 22, ISO/IEC teaches an image encoding apparatus comprising: filtering means for generating a plurality of sub-bands (low-pass and high-pass filter, section F.2), and applying hierarchical filtering to the sub-bands (levels are associated with each subband, section B.5); quantization means (Annex E) for dividing transform coefficients in the sub-bands, generated by said filtering means, with a quantization step size, weighted using weighting coefficients set from one subband to another, by way of performing quantization; code block generating means for splitting each sub-band following said quantization for generating a plurality of code blocks (section B.7) each being of a predetermined size (code block size is determined by precinct size, section B.7); bitplane generating means (Annex D) for generating a plurality of bitplanes (Fig. D-1) from the most significant bit to the least significant bit (section D.2.1), from one code block to another; bit modeling means (significance propagation; section D.3.1) for performing bit modeling from one bitplane to another (Fig. D-2 demonstrates the different bit models, using surrounding neighbor coefficients we are able to create a context vector that can predict different likely values in the bitplane); encoding pass generating means (selective arithmetic coding bypass, section D.6) for generating

encoding passes from one bitplane to another (Table D-9 teaches of the different types of passes with corresponding coding operations and bit-plane numbers); arithmetic coding means (arithmetic entropy coding, Annex C) for performing arithmetic coding in the encoding passes generated by said encoding pass generating means (Annex C); code volume controlling means (rate control, section J.14) for controlling the code volume, based on arithmetic codes, generated by said arithmetic coding means, so that a target code volume will be reached; and packet generating means (packet header information coding, section B.10) for appending a header to the arithmetic codes, controlled as to code volume by said code volume controlling means, to generate a packet (section B.10); said code volume controlling means summing said arithmetic codes in a sequence from the arithmetic code with the highest bit position to the arithmetic code with the lowermost bit (Fig. J-12), in the totality of the code blocks of said input picture, from one bitplane to another or from one code pass to another, said code volume controlling means halting the summation when a preset target code volume is exceeded (J.14).

As to claim 27, it differs from claim 22 in that claims 22 is an apparatus claim whereas claim 27 is a method claim. Therefore claim 27 is analyzed in the same way as claim 22.

As to claim 28, it differs from claim 22 in that claims 22 is an apparatus claim whereas claim 28 is a program. Therefore claim 28 is analyzed in the same way as claim 22.

As to claim 29, it differs from claim 22 in that claims 22 is an apparatus claim whereas claim 29 is a computer readable medium. Therefore claim 29 is analyzed in the same way as claim 22.

As to claim 2, ISE/IEC teaches wherein said encoding object predicting means counts the number of effective bitplanes, excluding zero bitplanes, for the totality of the code blocks in a frame in said input picture, and reference is made to a predetermined table, based on the count results, to find the number of bitplanes for encoding, from one frame to another (predicting could be interpreted two different ways. First, one may interpret predicting to be codestream termination, which is when we know how much bandwidth is available to us and terminating the codestream when the limit has been reached. This is in away predicting how much data we can compress. Annex D, section D.4 The second way is to interpret predicting as the region of interest. Then we are able to predict and know how much data to send or not to send by knowing the region of interest. Annex H).

As to claim 3, ISE/IEC teaches wherein said predetermined table is such a table in which the range of values of the effective bitplanes is correlated with the number of the bitplanes for encoding (Table D-9).

As to claim 4, ISE/IEC teaches wherein said encoding object predicting means counts the number of the effective bitplanes, excluding zero bitplanes, for the totality of the code blocks in the subbands of said input picture, and wherein reference is made to said predetermined table, based on the count results, to find the number of the bitplanes for encoding, from one sub-band to another (predicting could be interpreted two

different ways. First, one may interpret predicting to be codestream termination, which is when we know how much bandwidth is available to us and terminating the codestream when the limit has been reached. This is in away predicting how much data we can compress. Annex D, section D.4 The second way is to interpret predicting as the region of interest. Then we are able to predict and know how much data to send or not to send by knowing the region of interest. Annex H).

As to claim 5, ISE/IEC teaches wherein said predetermined table is such a table in which the range of values of the effective bitplanes is correlated with the number of bitplanes for encoding, from one subband to another (Table D-10 and Table D-11).

As to claim 17, ISE/IEC teaches wherein said code volume controlling means sums said arithmetic codes in the same bit position in a sequence from a subband of the lowermost range to a subband of the highest range (Fig. J-12).

As to claim 18, ISE/IEC teaches wherein said code volume controlling means sums said arithmetic codes in the same bit position in a sequence from a component of the luminance information to the component of the chroma information (Annex G teaches the use of luminance and chroma information).

As to claim 23, ISE/IEC teaches wherein said weighting coefficients are set so that the lower the frequency of the frequency component of a subband being quantized, the smaller is the quantization step size (Annex E teaches the process of quantization and the use of scalar coefficients).

As to claim 24, ISE/IEC teaches wherein said weighting coefficients are set so that the quantization step size is smaller for a component of the luminance information

than for a component of the chroma information (E.1.1.1 teaches the determination of quantization step size) .

As to claim 25, ISE/IEC teaches wherein said code volume controlling means sums said arithmetic codes of the same bit position in a sequence from a subband of the lowermost frequency to a subband of the highest frequency (layered bit-stream abstraction; J.14.2).

As to claim 26, ISE/IEC teaches wherein said code volume controlling means sums said arithmetic codes of the same bit position in a sequence from the component of the luminance information to the component of the chroma information (Rate-distortion optimization; J.14.3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over International Standard, Information technology – JPEG 2000 image coding system (ISO/IEC 15444-1).

As to claim 6, ISE/IEC teaches wherein, an image is inputted, the number of bitplanes for encoding, associated with the sub-band with the highest splitting level, which is in the low range in the horizontal direction and which is in the high range in the vertical direction, is set to zero (the above describes a quantization method, which is located in Annex E). ISE/IEC does not expressly disclose that the input picture is an interlaced picture. However, Examiner takes Official Notice that the interlaced pictures are well known in the art. It would have been obvious at the time of the invention was made to one of ordinary skill in the art to use an interlace picture in the quantization step since Examiner takes official notice that the use of interlaced images are well known in the art because it is a way of uploading pictures that can give the appearance of uploading images faster.

As to claim 7, ISE/IEC teaches wherein, an image is inputted, the number of bitplanes for encoding, associated with the subbands of the totality of splitting levels, which are in the low range in the horizontal direction and which are in the high range in

the vertical direction, is set to zero (the above describes a quantization method, which is located in Annex E). ISE/IEC does not expressly disclose that the input picture is an interlaced picture. However, Examiner takes Official Notice that the interlaced pictures are well known in the art. It would have been obvious at the time of the invention was made to one of ordinary skill in the art to use an interlace picture in the quantization step since Examiner takes official notice that the use of interlaced images are well known in the art because it is a way of uploading pictures that can give the appearance of uploading images faster.

As to claim 8, ISE/IEC teaches of a predetermined table (Annex D). ISE/IEC does not expressly disclose that is stored in a ROM (read-only memory). However, Examiner takes Official Notice that storing tables in ROM is well known in the art. It would have been obvious at the time of the invention was made to one of ordinary skill in the art to store a table in ROM since Examiner takes official notice that storing a table in ROM would not allow further modification to the table.

Response to Amendment

5. Applicant's response to the last Office Action, filed on November 14th, 2006 has been entered and made of record.

6. In view of the Applicant's arguments and amendments, the claim objections (claims 1 and 11), the rejection made under 35 U.S.C. 112 second paragraph (claims 2,4,6 and 7), and the rejection made under 35 U.S.C. 101 (claim 21) are expressly withdrawn.

Response to Arguments

7. In response to applicant's remark that ISO/IEC Annex D does not direct to **encoding**. It is noted that ISO/IEC teaches the encoding process in Annex D (Page 11, section 6).

8. In response to applicant's remark that ISO/IEC does not teach the predicted number of bitplanes **for encoding** are **extracted**. It is noted that ISO/IEC teaches the code-blocks bit-planes are scanned and Fig. D-1 is an example of such a scanned pattern. Thus each bitplane is extracted through the scanning process.

9. In response to applicant's remark that ISO/IEC does not teach generating means for **generating a plurality of bitplanes**. It is noted that ISO/IEC teaches encoder requirements and states Annex D teaches the encoding process (Page 11, section 6).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Claire Wang whose telephone number is 571-270-1051. The examiner can normally be reached on Mid-day flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 571-272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Claire Wang
04/30/2007

JOSEPH MANCUSO
SUPERVISORY PATENT EXAMINER